configurations can also be developed where number and type of gates are reduced. For this, the Boolean expressions of D and B are modified as follows.

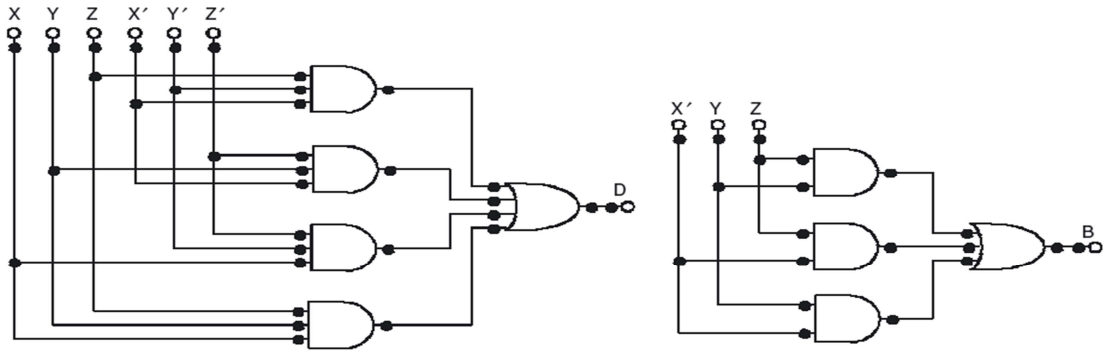


**Figure 4-11**

D = X′Y′Z + X′YZ′ + XY′Z′ + XYZ

= X′ (Y′Z + YZ′) + X (Y′Z′ + YZ)

= X′ (Y⊕Z) + X (Y⊕Z)′

= X⊕Y⊕Z

B = X′Z + X′Y +YZ = X′Y + Z (X′ + Y)

= X′Y + Z(X′Y + X′Y′ + XY + X′Y)

= X′Y + Z(X′Y + X′Y′ + XY)

= X′Y + X′YZ + Z(X′Y′ + XY)

= X′Y + Z(X⊕Y)′

Logic diagram according to the modified expression is shown in Figure 4.12.

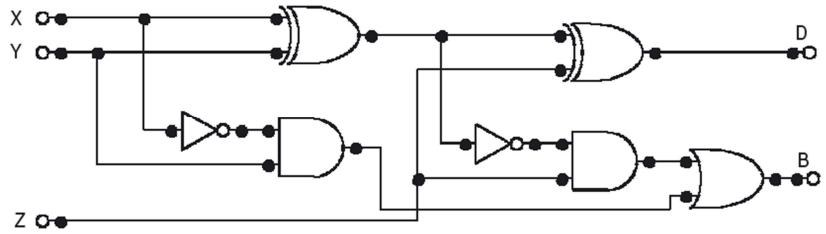


**Figure 4-12**

Note that the full-subtractor developed in Figure 4.12 consists of two 2-input AND gates, two 2-input XOR (Exclusive-OR) gates, two INVERTER gates, and one 2-input OR gate. This contains a reduced number of gates as well as type of gates as compared to Figure 4.12. Also, it may be observed, if compared with a half-subtractor circuit, the full-subtractor circuit can be developed with two half-subtractors and one OR gate.